IN THE CLAIMS:

1. (currently amended) A data processor, comprising:

a central processing unit; and

an address translation unit that receives virtual addresses output from the central processing unit and outputs physical addresses;

wherein the address translation unit includes a first translation lookaside buffer, a second translation lookaside buffer, and a control circuit for selecting one of the first and second translation lookaside buffers,

wherein the control circuit selectively controls operation ~~selects one~~ of the first and second translation lookaside buffers to selectively output a physical address based on stored enable information,

wherein the control circuit includes storage for storing the stored enable information and a selector coupled to outputs of the first translation lookaside buffer and the second translation lookaside buffer,

wherein the selector selectively operates to output the physical address based on the stored enable information,

wherein upon reset of the date processor the stored enable information controls the selector so that it does not output any physical address from either the first translation lookaside buffer or the second translation lookaside buffer,

wherein the address translation unit performs address translation in accordance with an area of a virtual address space of a virtual address received from the central processing unit.

2. (previously presented) A data processor according to claim 1,

wherein each of the first and second translation lookaside buffers has a plurality of entries for holding physical addresses associated with respective virtual addresses for performing the address translation,

wherein the central processing unit is capable of accessing a first virtual address space and a second virtual address space included in the virtual address space,

wherein the first translation lookaside buffer translates a virtual address of the first virtual address space to a physical address, and

wherein the second translation lookaside buffer translates a virtual address of the second virtual address space to a physical address.

7 6. (currently amended) A data processor, comprising:

a central processing unit; and

an address translation unit that receives virtual addresses output from the central processing unit and outputs physical addresses;

wherein the address translation unit includes a first translation lookaside buffer, a second translation lookaside buffer, and a control circuit for selecting one of the first and second translation lookaside buffers, wherein the control circuit selects one of the first and second translation lookaside buffers to output a physical address based on stored enable information,

wherein the address translation unit performs address translation in accordance with an area of a virtual address space of a virtual address received from the central processing unit,

wherein each of the first and second translation lookaside buffers has a plurality of entries for holding physical addresses associated with respective virtual addresses for performing the address translation,

wherein the central processing unit is capable of accessing a first virtual address space and a second virtual address space included in the virtual address space,

wherein the first translation lookaside buffer translates a virtual address of the first virtual address space to a physical address,

wherein the second translation lookaside buffer translates a virtual address of the second virtual address space to a physical address,

~~A data processor according to claim 2,~~

wherein first entries of the plurality of entries in the second translation lookaside buffer are controlled to be disabled from rewriting if the second translation lookaside buffer detects an address translation miss, and

wherein second entries of the plurality of entries in the second translation lookaside buffer are controlled to be enabled for rewriting if the second translation lookaside buffer detects an address translation miss.

8 7. (previously presented) A data processor according to claim 7,

wherein the first entries store physical addresses for an address translation miss handling routine.

9 8. (previously presented) A data processor according to claim ~~4~~ 8,

wherein it is determined whether or not the plurality of entries in the second translation lookaside buffer should be rewritten at an address translation miss in accordance with the address translation miss handling routine.

3 6. (previously presented) A data processor according to claim 1,

wherein the control circuit decodes upper bits of a virtual address output from the central processing unit and selects one of the first and second translation lookaside buffers in accordance with a decode result.

4 7. (previously presented) A data processor according to claim 1,

wherein the address translation unit further includes a selection circuit to which a first output of the first translation lookaside buffer and a second output of the second translation lookaside buffer are input, wherein the selection circuit selects one of the first and second outputs in accordance with a control signal of the control circuit.

5 8. (previously presented) A data processor according to claim 1,

wherein the address translation unit further includes an address chop circuit that fixedly forms a physical address from a virtual address when both of the first and second translation lookaside buffers are disabled.

6 9. (previously presented) A data processor according to claim 1,

wherein a page size of the first translation lookaside buffer is different from a size of the second translation lookaside buffer.

10. (currently amended) A data processor, comprising:

a central processing unit; and

an address translation unit that receives virtual addresses output from the central processing unit and outputs physical addresses;

wherein the address translation unit includes a first translation lookaside buffer, a second translation lookaside buffer, and a control circuit for selecting one of the first and second translation lookaside buffers, wherein the control circuit selects one of the first and second translation lookaside buffers to output a physical address based on stored enable information,

wherein the address translation unit performs address translation in accordance with an area of a virtual address space of a virtual address received from the central processing unit,

wherein each of the first and second translation lookaside buffers has a plurality of entries for holding physical addresses associated with respective virtual addresses for performing the address translation,

wherein the central processing unit is capable of accessing a first virtual address space and a second virtual address space included in the virtual address space,

wherein the first translation lookaside buffer translates a virtual address of the first virtual address space to a physical address,

wherein the second translation lookaside buffer translates a virtual address of the second virtual address space to a physical address,

~~A data processor according to claim 2,~~

wherein the number of the plurality of entries included in the first translation lookaside buffer is adapted so as to be larger than the number of the plurality of entries included in the second translation lookaside buffer, and

wherein a page size when the first translation lookaside buffer translates the virtual address of the first virtual address space to the physical address is adapted so as to be smaller than a page size when the second translation lookaside buffer translates the virtual address of the second virtual address space to the physical address.

11. (currently amended) A data processor, comprising:

a central processing unit; and

an address translation unit that receives virtual addresses output from the central processing unit and outputs physical addresses;

wherein the address translation unit includes a first translation lookaside buffer, a second translation lookaside buffer, and a control circuit for selecting one of the first and second translation lookaside buffers, wherein the control circuit selects one of the first and second translation lookaside buffers to output a physical address based on stored enable information, wherein the address translation unit performs address translation in accordance with an area of a virtual address space of a virtual address received from the central processing unit,

wherein each of the first and second translation lookaside buffers has a plurality of entries for holding physical addresses associated with respective virtual addresses for performing the address translation,

wherein the central processing unit is capable of accessing a first virtual address space and a second virtual address space included in the virtual address space,

wherein the first translation lookaside buffer translates a virtual address of the first virtual address space to a physical address,

wherein the second translation lookaside buffer translates a virtual address of the second virtual address space to a physical address,

~~A data processor according to claim 2,~~

wherein the address translation unit further includes a third translation lookaside buffer having a plurality of entries for holding predetermined physical addresses associated with predetermined virtual addresses for performing address translation, and

wherein the plurality of entries of the third translation lookaside buffer are capable of storing both a copy of a part of the entries of the plurality of entries in the first address buffer and a copy of a part of the entries of the plurality of entries in the second address buffer.

12. (previously presented) A data processor according to claim 11,

wherein the third address buffer is capable of operating selectively in accordance with an instruction fetch operation of the central processing unit so as to perform address translation processing in parallel with the first and second translation lookaside buffers.

13. (currently amended) A data processor, comprising:

a central processing unit; and

an address translation unit that receives virtual addresses output from the central processing unit and outputs physical addresses;

wherein the address translation unit includes a first translation lookaside buffer for performing address translation of a first virtual address space in the virtual addresses, a second translation lookaside buffer for performing address translation of a second virtual address space in the virtual addresses, and a control circuit for selecting one of the first and second translation lookaside buffers in accordance with whether a virtual address output from the central processing unit is in the first virtual address space or the second virtual address space,

wherein the control circuit selectively controls operation ~~selects one~~ of the first and second translation lookaside buffers to selectively output a physical address based on stored enable information

wherein the control circuit includes storage for storing the stored enable information and a selector coupled to outputs of the first translation lookaside buffer and the second translation lookaside buffer,

wherein the selector selectively operates to output the physical address based on the stored enable information,

wherein upon reset of the date processor the stored enable information controls the selector so that it does not output any physical address from either the first translation lookaside buffer or the second translation lookaside buffer.

14. (previously presented) A data processor according to claim 13,

wherein each of the first and second translation lookaside buffers includes a plurality of entries for holding physical addresses respectively associated with virtual addresses for performing address translation.

15. (previously presented) A data processor according to claim 13,

wherein the second translation lookaside buffer includes entries for an address translation miss handling routine of the first translation lookaside buffer, wherein the entries for the address translation miss handling routine are disabled from rewriting.

16. (currently amended) A design data module including information of a microprocessor module, comprising:

data for defining an address translation unit for receiving virtual addresses output from a central processing unit and outputting physical addresses,

wherein the address translation unit includes a first translation lookaside buffer, a second translation lookaside buffer, and a control circuit for selecting one of the first and second translation lookaside buffers,

wherein the address translation unit performs address translation in accordance with an area of a virtual address space of a virtual address received from the central processing unit,

wherein the control circuit selectively controls operation ~~selects one~~ of the first and second translation lookaside buffers to selectively output a physical address based on stored enable information

wherein the control circuit includes storage for storing the stored enable information and a selector coupled to outputs of the first translation lookaside buffer and the second translation lookaside buffer,

wherein the selector selectively operates to output the physical address based on the stored enable information,

wherein upon reset of the date processor the stored enable information controls the selector so that it does not output any physical address from either the first translation lookaside buffer or the second translation lookaside buffer.

17. (previously presented) A design data module according to claim 16,

wherein each of the first and second translation lookaside buffers has a plurality of entries for holding physical addresses associated with respective virtual addresses for performing the address translation,

wherein the central processing unit is capable of accessing a first virtual address space and a second virtual address space included in the virtual address space,

wherein the first translation lookaside buffer translates a virtual address of the first virtual address space to a physical address, and

wherein the second translation lookaside buffer translates a virtual address of the second virtual address space to a physical address.

18. (currently amended) A design data module including information of a microprocessor module, comprising:

data for defining an address translation unit for receiving virtual addresses output from a central processing unit and outputting physical addresses,

wherein the address translation unit includes a first translation lookaside buffer, a second translation lookaside buffer, and a control circuit for selecting one of the first and second translation lookaside buffers, wherein the address translation unit performs address translation in accordance with an area of a virtual address space of a virtual address received from the central

processing unit, wherein the control circuit selects one of the first and second translation lookaside buffers to output a physical address based on stored enable information,

wherein each of the first and second translation lookaside buffers has a plurality of entries for holding physical addresses associated with respective virtual addresses for performing the address translation,

wherein the central processing unit is capable of accessing a first virtual address space and a second virtual address space included in the virtual address space,

wherein the first translation lookaside buffer translates a virtual address of the first virtual address space to a physical address, and

wherein the second translation lookaside buffer translates a virtual address of the second virtual address space to a physical address,

~~A design data module according to claim 17,~~

wherein first entries of the plurality of entries in the second translation lookaside buffer are controlled to be disabled from rewriting if the second translation lookaside buffer detects an address translation miss, and

wherein second entries of the plurality of entries in the second translation lookaside buffer are controlled to be enabled for rewriting if the second translation lookaside buffer detects an address translation miss.

19. (new) A data processor according to claim 1, wherein the control circuit selectively activates the first and second address translation lookaside buffers, wherein power consumption of the data processor is selectively controlled.

20. (new) A data processor according to claim 10, wherein the control circuit selectively activates the first and second address translation lookaside buffers, wherein power consumption of the data processor is selectively controlled.